REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove. This Amendment is submitted in order to prepare this case for appeal.

Claims 1-4, 6-16, and 18-29 are pending and rejected. Claims 30-31 are added hereinabove. In addition, the Brief Description of the Drawings section of the Specification is amended hereinabove.

The Applicant respectfully traverses the drawing objection and related rejection of Claims 11, 23, and 27 under 35 U.S.C. 112, first paragraph. The Office Action asserts that the drawings don't show every feature of Claims 11, 23, and 27. Claim 11 recites a sleep mode voltage controller having a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage. The Applicant submits that FIG. 4 shows the sleep mode voltage controller features of Claim 11 and FIG. 5 shows a timing diagram of the circuit of FIG. 4 when the circuit of FIG. 4 is functioning in the embodiment discussed in Claim 11 and in paragraph 0030 of the Specification. Specifically, as stated in paragraph 0030, in the example embodiment the sleep mode voltage controller of FIG. 4 provides the array high supply voltage V_{ADD} at about 0.8 volts, the array low supply voltage V_{ASS} at about

0.4 volts and the n-well voltage V_{nwell} at about 1.2 volts for a general technology class of transistors. Thus, the SRAM array will have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell. FIG. 5 shows the well voltage such that an n-channel back bias voltage, a p-channel back bias voltage, and a voltage across the SRAM cell are about the same. For the embodiment described in paragraph 0030, the circuit of FIG. 4 works in the manner recited in Claim 11.

Similarly, Claim 23 recites a method of providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage. The Applicant submits that FIG. 4 shows the sleep mode voltage controller that performs the method of Claim 23, and FIG. 5 shows a timing diagram of the circuit of FIG. 4 when the circuit of FIG. 4 is functioning in the embodiment discussed in Claim 23 and in paragraph 0030 of the Specification. Specifically, as stated in paragraph 0030, in the example embodiment, the sleep mode voltage controller of FIG. 4 provides the array high supply voltage V_{ADD} at about 0.8 volts, the array low supply voltage V_{ASS} at about 0.4 volts and the n-well voltage V_{nwell} at about 1.2 volts for a general technology class of transistors. Thus, the SRAM array will have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell. FIG. 5 shows the well voltage being provided in accordance with the method of Claim 23 such that an n-channel back bias voltage, a p-channel back

bias voltage, and a voltage across the SRAM cell are about the same (i.e. all about 0.4 volts).

Claim 27 recites that the sleep mode voltage controller provides the array low supply voltage V_{ASS} higher than a substrate voltage during said sleep mode. The Applicant submits that FIG. 5 clearly shows the array low supply voltage V_{ASS} higher than the substrate voltage $V_{substrate}$.

The Applicant also respectfully traverses the statement in the Office Action that the "claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." The Applicant submits that "one skilled in the relevant art" could have understood the function of the circuit of original FIG. 2 and how it could have functioned as described in the original Specification (such as original paragraphs 0027, 0028, and 0030 plus Claims 11, 23, and 27) without the aid of FIGS. 4 and 5 (which were added to explain the invention to the Examiner – but are not needed to explain the invention to "one of ordinary skill in the art").

In addition, the Applicant respectfully traverses the statement in the Office Action that the "[n]ewly added Fig. 5 was not described in the original specification." The Applicant submits that Fig. 5 is supported by paragraphs

0027, 0028, and 0030 of the original Specification plus original Claims 11, 23, and 27.

Furthermore, the Applicant respectfully traverses the statement in the Office Action that "Fig. 5 shows the voltage across the cell clearly higher than the back bias on p-channel and also higher than the back bias n-channel; and the low operating voltage is clearly the same as the Vsubstrate." The Applicants submits that, as stated in paragraph 0030, Fig. 5 shows that the sleep mode voltage controller may provide the array high supply voltage V_{ADD} at about 0.8 volts, the array low supply voltage V_{ASS} at about 0.4 volts and the n-well voltage V_{nwell} at about 1.2 volts for a general technology class of transistors. Thus, the SRAM array may have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell. Therefore, this embodiment provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage, and a voltage across the SRAM cell are all about the same (all about 0.4 volts).

Independent Claim 1 positively recites that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant respectfully traverses the statement in the Office Action (page 4) that V_{DDM} of Deng et al. is the advantageously claimed array high supply voltage V_{ADD}. The Applicant submits that Deng et al. labels the array high voltage supply V_{DDA} (column 2 lines 48-49); therefore, it is not element V_{DDM} in the cited lines of columns 5 and 6. As a result, the Office Action argument incorrectly confuses the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al.

The Applicant also respectfully traverses the statement in the Office Action (pages 4-5) that the inherent voltage drop of the SRAM transistors is the advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the parameter, but it is not the parameter. The Applicant notes that the definition of the term "transistor parameter" is described in the Specification (paragraphs 0029, 0030, 0031, 0037).

Regarding Claims 2-4, the Applicant repeats the assertion that the Office Action argument (page 5) incorrectly confuses the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Plus the Office Action argument (page 5) incorrectly confuses the high operating voltage (V_{DDM}) of Deng et al. with the advantageously claimed array high supply

voltage V_{ADD}. The same can be said for the Office Action argument (page 5) concerning V_{SSM} of Deng et al. Moreover, the Applicant respectfully traverses the statement in the Office Action (page 5) that the "sleep mode power down voltage controller 170 provides the high supply voltage VDDM and the low supply voltage VSSM relative to the n-well voltage to SRAM array 100" (emphasis omitted). The Applicant asserts that Deng et al. does not teach that V_{SSM} or V_{DDM} is specified relative to a well voltage. Rather, when the n-well changes value neither V_{SSM} nor V_{DDM} will follow (column 5 lines 58-65, FIG. 1).

Furthermore, regarding Claim 4, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n-well voltage at about high operating voltage VDD of 1.2 V" is not the same as a well voltage at about V_{DD} during sleep mode as advantageously claimed.

Regarding Claims 12 and 13, the Applicant respectfully traverses the assertion (Office Action page 5) that Deng et al. teaches that the sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a minimum voltage across the SRAM array that is sufficient for data retention and minimizing a total leakage current. Deng et al. does not teach minimizing leakage current while retaining data (column 2 lines 27-31).

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over Deng et al. Furthermore, Claims 2-4 and 6-13 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 14 positively recites that providing the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} is based on a transistor parameter of at least one transistor of the SRAM array. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant respectfully traverses the statement in the Office Action (page 4) that V_{DDM} of Deng et al. is the advantageously claimed array high supply voltage V_{ADD}. The Applicant submits that Deng et al. labels the array high voltage supply V_{DDA} (column 2 lines 48-49), not element V_{DDM} in the cited lines of columns 5 and 6. Therefore, the Office Action argument incorrectly confuses the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al.

The Applicant also respectfully traverses the statement in the Office Action (pages 4-5) that the inherent voltage drop of the SRAM transistors is the

advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the parameter, but it is not the parameter. The Applicant notes that the definition of the term "transistor parameter" is described in the Specification (paragraphs 0029, 0030, 0031, 0037).

Regarding Claims 15-16, the Applicant repeats the assertion that the Office Action argument (page 5) incorrectly confuses the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al. Plus the Office Action argument (page 5) incorrectly confuses the high operating voltage (V_{DDM}) of Deng et al. with the advantageously claimed array high supply voltage V_{ADD}. The same can be said for the Office Action argument (page 5) concerning V_{SSM} of Deng et al. Moreover, the Applicant respectfully traverses the statement in the Office Action (page 5) that the "sleep mode power down voltage controller 170 provides the high supply voltage VDDM and the low supply voltage VSSM relative to the n-well voltage to SRAM array 100" (emphasis omitted). The Applicant asserts that Deng et al. does not teach that V_{SSM} or V_{DDM} is specified relative to a well voltage. Rather, when the n-well changes value, V_{SSM} and V_{DDM} will not follow (column 5 lines 58-65, FIG. 1).

Furthermore, regarding Claim 16, the Applicant respectfully submits that the statement in the Office Action (page 4) that "n-well voltage at about high

operating voltage VDD of 1.2 V" is not the same as a well voltage at about V_{DD} during sleep mode as advantageously claimed.

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over Deng et al. Furthermore, Claims 15-16 and 18-23 are allowable for depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 24 positively recites that sleep mode voltage controller provides the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are based on a transistor parameter of at least one transistor of the SRAM array. In addition, Claim 24 recites modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to said sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Deng et al. (column 6 lines 16-42).

The Applicant respectfully traverses the statement in the Office Action (page 4) that V_{DDM} of Deng et al. is the advantageously claimed array high supply voltage V_{ADD}. The Applicant submits that Deng et al. labels the array high voltage supply V_{DDA} (column 2 lines 48-49) and it is not element V_{DDM} of the cited lines in columns 5 and 6. Therefore, the Office Action argument incorrectly

confuses the array high voltage supply (V_{DDA}) of Deng et al. with the high operating voltage (V_{DDM}) of Deng et al.

The Applicant also respectfully traverses the statement in the Office Action (pages 4-5) that the inherent voltage drop of the SRAM transistors is the advantageously claimed transistor parameter. The Applicant submits that the inherent voltage drop of an SRAM transistor is an inherent response to the parameter, but it is not the parameter. The Applicant notes that the definition of the term "transistor parameter" is described in the Specification (paragraphs 0029, 0030, 0031, 0037).

Moreover, Deng et al. does not teach modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to said sleep mode, as advantageously claimed (column 2 lines 47-64, FIG. 1).

Regarding Claim 25, the Applicant respectfully traverses the assertion (Office Action page 5) that Deng et al. teaches the advantageously claimed modification of the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to said sleep mode. Deng et al. does not teach the advantageously claimed modification (column 2 lines 47-64, FIG. 1).

Regarding Claim 27, the Applicant respectfully traverses the statement in the Office Action (pages 5-6) that "it is very well known in the art that in any memory integrated circuit the base substrate voltage must be lower than any operating power supply voltage during any operation." The Applicant submits that the lowest operating power supply may be lower than the base substrate voltage in order to provide a forward bias (i.e. to lower Vt's for material at the slow process corner).

Therefore, the Applicant respectfully traverses the Examiner's rejection of Claim 24 and respectfully asserts that Claim 24 is patentable over Deng et al. Furthermore, Claims 25-29 are allowable for depending on allowable independent Claim 24 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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